Muhammad (Abid) **Abdullah**

itsabdullah.dev | 617-955-2835
mabdullah@alum.mit.edu | github.com/abdullah8a0

Education

Massachusetts Institute of Technology
B.S. in Computer Science and Engineering **Class of 2024**
- *Selected Coursework*: Computer Architecture (Graduate), Advanced Algorithms (Graduate), Performance Engineering, Systems Engineering, Software Construction, Distributed Systems, Theory of Computation

B.S. in Mathematics **Class of 2024**
- *Selected Coursework*: Linear Algebra, Probability, Information Theory, Differential Eqs, Real Analysis, Topology

Projects

OneChan: An FPGA-based Chess Engine supplemented with a custom basic TPU. link
U2F: An open-source, homemade 2-factor authentication security key based on the FIDO alliance's U2F specification link
Profemon: A dynamic, PVP, in-person, turn-based fighting game similar to Pokemon Go. Implemented on an ESP32 link
Optimal Bounds For Range Search: Reviewed and simplified several recent keystone papers in DS and Algorithms. link

Awards

International Mathematical Olympiad 2020 (IMO) - Honorable Mention
6.172 (Performace Engineering) Leiserchess Tournament 2022 - Placed 1st
6.004 (Computation Structures) MNIST Hardware Acceleration final project - Placed 2nd

Work Experience

Siemens EDA DISW Jun. 2024 - present
R&D Software Engineer ***Wilsonville, OR***

- → Lead performance engineering efforts for Siemens' Sequential Logic Equivalence Checking (SLEC) Engine, the performance-critical backend powering formal verification tools widely deployed across semiconductor and hardware design industries. Leveraged template metaprogramming optimizations and assembly-level performance tuning, with particular focus on optimizing hot paths in core verification algorithms.
- → Architected and implemented novel ordering strategies for CCoverCheck code coverage product, employing advanced data structures and custom memory layouts to reduce SAT solver calls by 22%.
- → Spearheaded the removal of redundant engine parameters, decreasing their count from 3000+ to 250, greatly simplifying internal bookkeeping.

Harvard SEAS Summer 2023
Student Researcher ***Cambridge, MA***

- → Developed a novel approach for detecting microarchitectural side-channel vulnerabilities using staged interpreters and formal methods. Implemented a collapsing tower of interpreters in Scala that transforms hardware timing behaviors into analyzable C code, enabling detection of Spectre-like vulnerabilities through bounded model checking.
- → The technique successfully identified cache-based and speculative execution timing attacks while maintaining composability of hardware features. Published in PEPM 2025. Short paper

MIT Computer Architecture Lab Jan. 2022 - May 2023
Morais and Rosenblum Undergraduate Research Scholar ***Cambridge, MA***

- → Implemented a modified KVM module in the Linux kernel to support Trusted Execution Environments (TEEs) for RISC-V, focusing on secure memory isolation between VMs and the host OS
- → Leveraged RISC-V PMP specification to enable fine-grained memory access control and integrity verification across kernel privilege levels (U-mode, S-mode, H-mode, M-mode)
- → Built trap handlers and security monitors to protect against page table manipulation attacks while maintaining performance

Rescale, Inc. Summer 2022
SW Intern ***San Franciso, CA***

- → Implemented an example Data Analysis pipeline to showcase cloud management systems. Wrote tutorials for new users on best practices for cloud HPC deployments on the company platform. Conducted platform reviews and offered recommendations to company teams.

Skills Summary

Languages: *Software*; C++, Python, C, Typescript, Scala, x86-Assembly, RISC-V. *Hardware*; System Verilog, Bluespec
Tools: Git, Linux, LLVM, clang, cilk, Xilinx SDK, React, Angular, gdb, Valgrind, Z3, yosys
Interests: Performance Engineering, Hardware/Software co-design, Computer Architecture, Formal Methods